## IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A method for graphically tracking a progression of instructions through one or more hardware components, comprising:

defining a plurality of graphical icons for a plurality of instructions of a code segment, each of the plurality of graphical icons having a displayable appearance that identifies a type of instruction;

tracking each of the plurality of graphical icons when simulating execution of the code segment through the one or more hardware components by generating a graphical display of a plurality of execution pipelines, each of which has indicia associated therewith that differs from the indicia associated with the remaining pipelines of said plurality of execution pipelines and placing a subset of said plurality of graphical icons adjacent to a first sub-portion of said indicia associated with one of said plurality of execution pipelines; and

displaying a progression of each of the plurality of graphical icons through the one or more hardware components during the execution of the code segment by sequentially placing graphical icons of said subset adjacent to additional sub-portions of said indicia associated with said one of said plurality of execution pipelines.

2. (Currently Amended) The method of claim 1, wherein ~~the plurality of instructions define a group of instructions, and each instruction in the group of instructions being processed in order defined by the code segment~~ each of the icons of said subset having said displayable appearance with characteristics matching a characteristic of indicia associated with said one of plurality of execution pipelines and distinguishable from characteristics of

indicia associated with the remaining execution pipelines of said plurality of execution pipelines, when placed adjacent thereto.

3. (Currently Amended) The method of claim 2, wherein ~~processing the group of instructions in order enables display of first processed instructions through later hardware stages of the one or more hardware components and enables simultaneous display of later processed instructions through earlier hardware stages of the one or more hardware components~~ wherein said sub-portion and said additional sub-portions define multiple sub-portions, each of which corresponds to a clock cycle that differs from a clock cycle corresponding to the remaining sub-portions of said multiple sub-portions.

4. (Currently Amended) The method of claim 1, wherein ~~the method operation of~~ displaying the progression of each of the plurality of graphical icons includes,

displaying a tabular view of the progression of each of the plurality of graphical icons through the one or more hardware components during the execution of the code segment.

5. (Original) The method of claim 1, further comprising,

selecting the plurality of graphical icons to cause displays of information associated with the plurality of graphical icons.

6. (Original) The method of claim 5, wherein the information is defined by one or more of a name of the instruction, an internal representation of the instruction, a program counter associated with an instruction, a physical memory location of the instruction, an instruction disassembly, a register source, a register destination, a virtual addresses of data, and a physical address of the data to be loaded.

7. (Original) The method of claim 1, wherein the displayable appearance is defined by one or more of a geometric shape, a shading, a pattern, an alphanumeric character, a symbol, and a color.

8. (Original) The method of claim 1, wherein the progression is movement between the one or more hardware components through intervals of time.

9. (Original) The method of claim 1, wherein the method operation of tracking each of the plurality of graphical icons includes,

monitoring the plurality of graphical icons entering into the one or more hardware components; and

monitoring the plurality of graphical icons departing from the one or more hardware components.

10. (Original) The method of claim 1, wherein the one or more hardware components is defined by one or more of an instruction buffer, an integer instruction execution pipeline, a loads and stores execution pipeline, a branch execution pipeline, a floating point add execution pipeline, a floating point multiply execution pipeline, a microprocessor, an address switch, a data switch, a memory controller, an Ethernet, a network, a data cache, a memory, a bus, an interconnect, a motherboard routing, and a protocol.

11. (Original) The method of claim 1, wherein the execution of the code segment generates the instructions to the one or more hardware components.

12. (Original) The method of claim 1, wherein the plurality of instructions of the code segment are defined by one or more of a load instruction, an add instruction, a subtract instruction, a store instruction, a branch instruction, a register movement instruction, a shift instruction, an input instruction, and an output instruction.

13. (Currently Amended) A computer readable medium having program instructions for graphically tracking a progression of instructions through one or more hardware components, comprising:

program instructions for defining a plurality of graphical icons for a plurality of instructions of a code segment, each of the plurality of graphical icons having a displayable appearance that identifies a type of instruction;

program instructions for tracking each of the plurality of graphical icons when simulating execution of the code segment through the one or more hardware components by generating a graphical display of a plurality of execution pipelines, each of which has indicia associated therewith that differs from the indicia associated with the remaining pipelines of said plurality of execution pipelines and placing a subset of said plurality of graphical icons adjacent to a first sub-portion of said indicia associated with one of said plurality of execution pipelines; and

program instructions for displaying a progression of each of the plurality of graphical icons through the one or more hardware components during the execution of the code segment by sequentially placing graphical icons of said subset adjacent to additional sub-portions of said indicia associated with said one of said plurality of execution pipelines.

14. (Currently Amended) The computer readable medium of claim 13, wherein ~~the plurality of instructions define a group of instructions, and each instruction in the group of instructions being processed in order defined by the code segment~~ said program instruction for defining further includes a sub-routine to provide each of the icons of said subset with said displayable appearance having characteristics matching a characteristic of indicia associated with said one of plurality of execution pipelines and distinguishable from characteristics of indicia associated with the remaining execution pipelines of said plurality of execution pipelines, when placed adjacent thereto.

15. (Currently Amended) The computer readable medium of claim 14, wherein ~~processing the group of instructions in order enables display of first processed instructions through later hardware stages of the one or more hardware components and enables simultaneous display of later processed instructions through earlier hardware stages of the one or more hardware components~~ wherein said sub-portion and said additional sub-portions define multiple sub-portions and further including a sub-routine to correspond each of said multiple sub-portions with a clock cycle that differs from a clock cycle corresponding to the remaining sub-portions of said multiple sub-portions.

16. (Original) The computer readable medium of claim 13, wherein the program instructions for displaying a progression of each of the plurality of graphical icons includes,

program instructions for displaying a tabular view of the progression of each of the plurality of graphical icons through the one or more hardware components during the execution of the code segment.

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17. (Original) The computer readable medium of claim 13, further comprising,

program instructions for selecting the plurality of graphical icons to cause displays of information associated with the plurality of graphical icons.

18. (Original) The computer readable medium of claim 17, wherein the information is defined by one or more of a name of the instruction, an internal representation of the instruction, a program counter associated with an instruction, a physical memory location of the instruction, an instruction disassembly, a register source, a register destination, a virtual addresses of data, and a physical address of the data to be loaded.

19. (Original) The computer readable medium of claim 13, wherein the displayable appearance is defined by one or more of a geometric shape, a shading, a pattern, an alphanumeric character, a symbol, and a color.

20. (Original) The computer readable medium of claim 13, wherein the progression is movement between the one or more hardware components through intervals of time.

21. (Original) The computer readable medium of claim 13, wherein the program instructions for tracking each of the plurality of graphical icons includes,

program instructions for monitoring the plurality of graphical icons entering into the one or more hardware components; and

program instructions for monitoring the plurality of graphical icons departing from the one or more hardware components.

22. (Original) The computer readable medium of claim 13, wherein the one or more hardware components is defined by one or more of an instruction buffer, an integer instruction execution pipeline, a loads and stores execution pipeline, a branch execution pipeline, a floating point add execution pipeline, a floating point multiply execution pipeline, a microprocessor, an address switch, a data switch, a memory controller, an Ethernet, a network, a data cache, a memory, a bus, an interconnect, a motherboard routing, and a protocol.

23. (Original) The computer readable medium of claim 13, wherein the execution of the code segment generates the instructions to the one or more hardware components.

24. (Original) The computer readable medium of claim 13, wherein the plurality of instructions of the code segment are defined by one or more of a load instruction, an add instruction, a subtract instruction, a store instruction, a branch instruction, a register movement instruction, a shift instruction, an input instruction, and an output instruction.